CoOperate™

The Power to Bring All Simulation Components Together
Into *Your* System's Model
A Unified Simulation™ Component

A software library that turns one or more Instruction Set Simulator (ISS) processor models into a synchronized co-simulating model.

Capable of cycle-accurate synchronization between multiple disparate ISS models and HDL simulators

Significantly reduces connectivity complexity between multiple ISS models and VHDL and Verilog models

Represents a breakthrough in capability and connectivity versus cost

Enables pre-silicon software development

CoOperate Enables Any Hardware and Software Simulators to Become a Winning Team

CoOperate is a dynamic library that provides a simple interface for synchronizing multiple software and hardware simulators together into a single system model. CoOperate turns a set of ISS models into a co-simulating model, complete with hardware/software model synchronization, inter-process control, multicore control and the high performance you've come to expect from our Unified Simulation products.

CoOperate Turns ISS Models Into a Co-Simulating Model

CoOperate is designed for pin-aware cycle-accurate processor models like Precyse. By adding just a few simple function calls in an ISS model, CoOperate provides a fast and reliable interface to most Verilog and VHDL-based simulators.

Plus, with an optional bus model, CoOperate can transform transaction-based ISS models, too. With CoOperate, the precision represented by the ISS is accurately reflected in the co-simulation results.

A Valuable Tool for Hardware and Software Developers

CoOperate's value for hardware developers lies in its simplicity. Just start your CoOperate-ready HDL design and CoOperate initializes and automatically establishes synchronized connections with all ISS models involved—without the clumsiness of an additional tool in your tool chain.

CoOperate's value to software developers lies in efficiency. Software developers are finally able to develop *and test* their drivers and applications in parallel with the current SoC configuration the hardware designers are using. This means no stubs in their code for missing devices—they can begin to debug their final, unmodified software, not just pre-silicon, but during hardware verification.

CoOperate-enhanced models make more than sense—they make schedules.

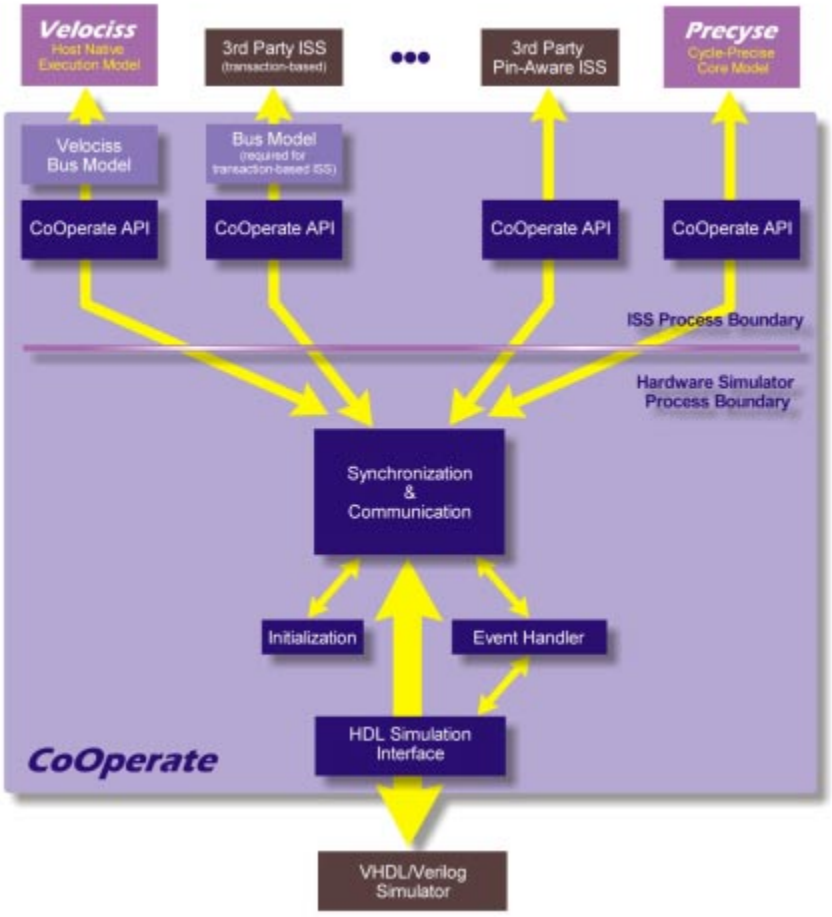
CoOperate-Enhanced Co-Simulating Models Synchronize With Industry Standard Hardware Simulators

Verilog. VHDL. SystemC. Mixed language. CoOperate supports virtually

all industry standard hardware simulators. Moreover, CoOperate provides a high throughput conduit through which data can flow from the software model or models to the HDL simulator and back, with full synchronization for synchronous and asynchronous events.

CoOperate's Co-Simulating Models Provide Big Benefits in a Streamlined Package

CoOperate connects one or more ISS models to an HDL simulator as efficiently as possible. In doing so it provides synchronization accuracy equal to the accuracy of the ISS models it is connecting—if they are cycle-accurate, so is CoOperate. Moreover, the ISS models can communicate directly to each other, connecting through any exposed pins or busses. Thus, CoOperate has value even if no hardware simulation is necessary. Further, CoOperate can concurrently interface with ISS models on Solaris, Windows, and Linux. With CoOperate, virtually any model of any processor core can now be used to test your system design and application software.



CoOperate is a crucial part of a multicore design, since it easily connects to and synchronizes processor models from different vendors, even when those models run on different operating systems. CoOperate provides a high performance communication path amongst each ISS model as well as a hardware simulator. Moreover, it is not limited to a specific Verilog simulator, as a simple PLI interface would be. Rather, CoOperate interacts with all major Verilog and VHDL simulators simply, efficiently, and accurately.

Further, CoOperate is a performance leader. While it is true that it doesn't have all the "optimizations" of other co-simulation tools, it does provide an optimized communication path so that data transferred between the simulators—often thousands of times a second—is handled as efficiently as possible. This results in the fastest possible co-simulation speeds—as much as 5 *times* faster than those other tools, in standard mode.

Finally, CoOperate co-simulating models are cost leaders. We believe that you shouldn't have to seek another round of funding to provide your systems engineers with state-of-the-art tools. CoOperate is priced like a model.

CoOperate is One Component of Unified Simulation, Our SoC Multicore System Engineering Environment

Find out more about Unified Simulation, an advanced environment designed to address multiprocessor system-on-chip co-design and verification bottlenecks. If you are a core designer, call to see how Endeavor can partner with you to provide modeling solutions, including CoOperate-enhanced co-simulating models, for you and your customers.

Please Contact:

ENDEAVOR INTERTECH CORPORATION

PO Box 744
Hillsboro, Oregon 97123

Telephone: (503) 628-6200
Fax: (503) 628-1155
email: sales@endeav.com
web: www.endeav.com