



**System-on-Chip
co-verification ready
processor models that are:**

*Cycle and Pin Accurate—
verified on every clock cycle or
subcycle*

*High Performance—simulation
speeds of 1,000-10,000 times
the performance of an RTL
model*

*Supports Multiple Cores—fully
synchronizes homogeneous or
heterogeneous cores and
multiple clock domains*

**Precision. Speed. Flexibility. Just
As a Soccer Team Depends on the
Goal Keeper, Your Design Team
Depends On the Tools. Average is
Simply Not Good Enough.**

Precyse is a processor model based in C++ that, like a great keeper in soccer, exhibits extraordinary abilities and performance.

For example, Precyse maintains the precision necessary to instill confidence in co-verification, and the accuracy to assure application and systems software—from algorithm to interrupt handlers—are golden. Precyse also significantly speeds validation of SoC designs, by providing precise timing, data paths and synchronization between internal and external models.

**A Great Keeper Makes the
Complex Appear Simple. Like
Precyse's Multicore Simulations.**

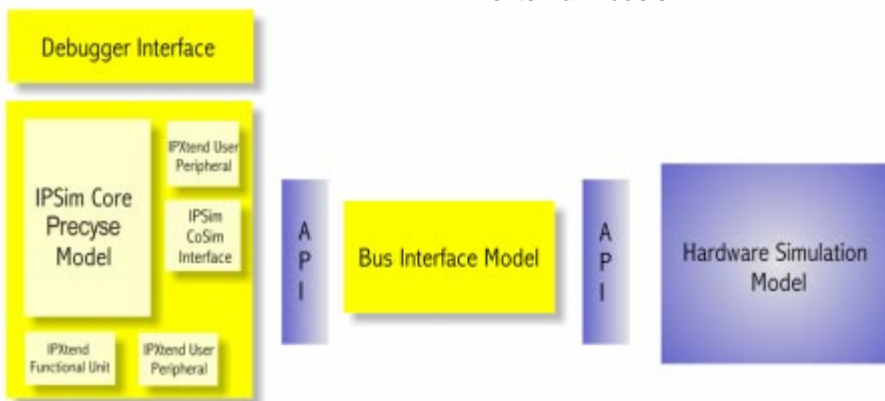
Complex core designs often combine multiple IP, such as a microprocessor core with a DSP. Every Precyse model has built in multiprocessor support, so you can simulate such a design almost as easily as starting another debugger process. There is no need to develop spurious glue logic who's only value is synchronizing the clocks because Precyse's IPSim kernel handles it all for you.

The IPSim kernel can precisely mesh cores of different clock domains, even non-multiples of each other. Each core maintains its own state and debugger, and each debugger automatically coordinates with the others.

**A Great Keeper's Precision Saves
the Day. Precyse's Clock-Cycle
Accuracy is Just Right for the Job.**

Precyse simulators are a natural for working edge-to-edge with hardware simulators, because we maintain strict cycle or sub-cycle accuracy. At every clock edge, all our simulated pins and busses have the same values as the hardware.

Those that have been unimpressed by co-verification's performance may find that it had to do with the quality of the models that were available. Many models that are billed as being "cycle-close" are misleading. Precyse gives



**Precyse Processor Model
with IPSim Kernel**

Precyse is designed from the start to be an integral part of the EDA design flow. Whether used in hardware/software co-verification as shown above, co-design, or middleware development, Precyse models bridge the gaps in conventional tools with superior performance, accuracy, and integration.

you the assurance that validation really means something. More than the *hope* you might get from a close ISS; Precyse gives you *confidence*.

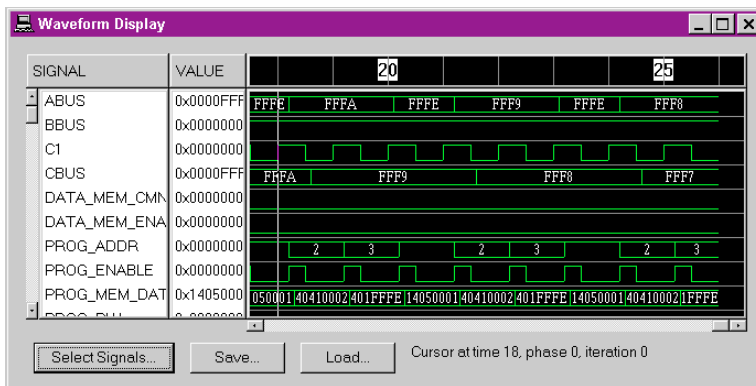
Precyse Assists in Hardware Verification

Often, the best test case to verify SoC hardware is your full application—if you have a model that can run fast enough. Precyse enables successful verification of even difficult-to-test hardware components. With speeds averaging 400,000 instructions per second, you can execute fast enough to get to the critical section of code that affects the component in question, then drop into the HDL to debug the hardware. All in a fraction of the time it takes using an RTL simulation, and without giving up significant accuracy.

A Keeper's Flexibility Transforms Common Into Remarkable. IPXtend™ Provides Plug-in Support for Core Extensions.

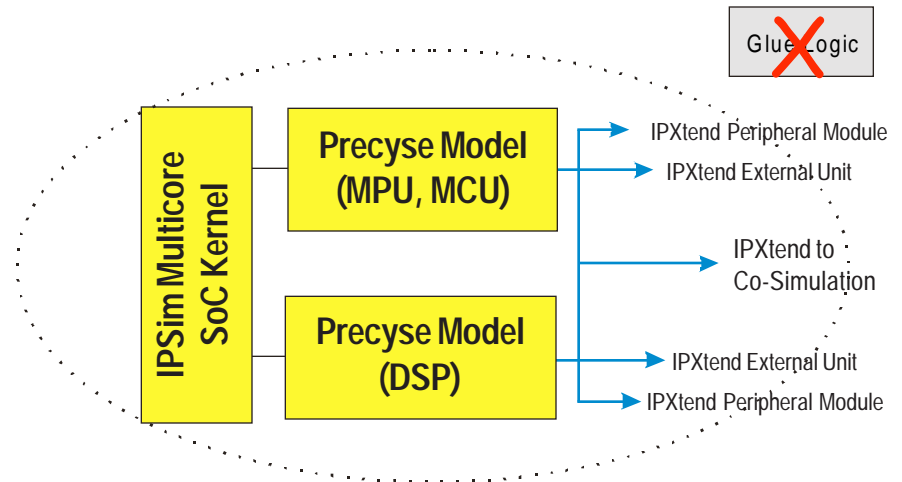
A typical ISS has limited value as soon as the customer extends the core into a chip by adding I/O or a specialized processor—because the ISS can't be easily enhanced. Precyse models, through our IPXtend plug-in API, provide the ability for our customers to add new modules to make it reflect the *final* design.

With IPXtend, users have a template with instructions for filling it out. Once the new component is complete, Precyse will seek out newly registered components and integrate their execution into the normal functioning of the tool.



IPSim Precyse's unique waveform generator allows hardware designers to compare generated signals with the hardware, and software developers to inject interrupts on the exact cycle for testing and debugging purposes.

GlueLogic



Precyse models are created in the same manner as SoC hardware design—a core to which additional peripherals and functional units can be attached to represent a complete chip. Precyse can even simulate complex multi-processor designs (as shown above), while remaining co-simulation capable.

The Quickness of a Great Keeper Delivers Significant Results. So Too With Precyse.

Precyse significantly speeds validation of SoC designs—especially complex multicore designs—by providing precise timing, data paths and synchronization between internal and external models. Precyse customers can verify significant portions of critical software in a fraction of the time now spent. This means a new design will cost less, and be to market quicker.

Precyse is One Component of Unified Simulation, Our SoC Multicore System Engineering Environment

Find out more about Unified Simulation, an advanced environment designed to address multiprocessor system-on-chip co-design and verification bottlenecks. If you are a core designer, call us to see how Endeavor can partner with you to provide modeling solutions, including Precyse cycle-precise models, for you and your customers.

Please Contact:

Endeavor Intertech Corporation
PO Box 744
Hillsboro, Oregon 97123

Telephone: (503) 628-6200
Fax: (503) 628-1155
email: sales@endeav.com
web: www.endeav.com