ENDEAVOR INTERTECH CORPORATION

Custom Bus Model Development and Integration

Endeavor is experienced in developing entire turn-key Bus Models for the leading Co-verification environments.

We are especially proud of our close, collaborative association with the Synopsys Eaglei® Hardware/Software Co-Verification Team

Bus Models are the Critical Link Between HW & SW Simulation in Co-Verification; Choose Your Designer Carefully

The rapidly growing demand for System-on-Chip (SoC) devices and the associated acceleration of time to market has vaulted hardware/software integration into one of the most essential components of embedded systems development.

Co-verification is the process of bridging the software development world and its abstracted simulation to the gates-and-transistors HDL simulation world. Co-verification is critical for eliminating defects early in the product's development process.

The crucial link that bridges these two worlds is the bus functional model, also called the bus interface model. Given the critical nature of such models, it is essential that it be developed by an expert with an understanding of the hardware, expertise in the two simulation worlds, knowledge of specific issues relating to the EDA environment and skill developing the workings of the bus model. Endeavor's vast experience gives us that perspective.

When We Model a Bus, We Model Everything

A bus model is not a good place to cut corners. In fact, because of its critical task of synchronizing the two simulation worlds both temporally and spatially, it had *better* be complete. Endeavor has the experience and knowledge to make sure they are fully functional; fully accurate.

For example, integrating the spatial components means allowing the HW and SW worlds to "touch". This generally involves providing a useful abstraction of address spaces and the buses used to carry out accesses to those spaces. It must be pin-list compatible and fully interchangeable with HDL interfaces.

Temporally, the bus model must insure correct sequencing and timing for every bus request, every interrupt, every reset, and every possible single- or multi-cycle event.

Co-Verification is Only as Accurate as Each Component, Including the Bus Models

For Co-verification to be valuable, every component—especially the bus model—must themselves be accurate. Endeavor bus models are tested by generating a series of HDL designs that inject specific stimuli—simple cases as well as complex multiple stimuli—to the pins on the bus. Then we compare the generated bus waveforms against the hardware manufacturer's specification to guarantee accuracy.

Thus, co-verification with an Endeavor bus model gives you the assurance that validation really means something. It's the confidence that comes from knowing your integration problems are ironed out before synthesis.

The bus model is the critical tool in co-verification for synchronizing the spatial and temporal components of hardware and software simulation

High Performance, Cycle Accurate Simulators: the Natural Complement to Bus Model Development

The best complement to an Endeavor bus model is an IPSim™ software simulator. IPSim is Endeavor's high precision, high performance software instruction set simulator. IPSim is more than your standard ISS, however, because aside from running at 100,000 to 400,000 instructions per second, it is 100% cycle and pin accurate.

More than that, IPSim is extensible by the user, and therefore a perfect complement to the way designers create SoC architectures—with cores. With IPSim, Endeavor customers can turn a core simulator into a chip simulator quickly, easily, and without additional expense.

Finally, IPSim is designed to work in co-verification environments, and naturally interfaces to bus models. That is one reason why Synopsys chose to collaborate with Endeavor to build IPSim ISSs and bus models directly for the Eaglei Co-Verification division. Let us provide you with the same confidence industry leaders like Synopsys enjoy.

Enable the Largest Potential Market Possible—Support All Co-Verification Environments Now

Endeavor can help. We are familiar with most of the popular co-verification environments in use today, including Synopsys Eaglei, Mentor Graphics Seamless, Cadence Affirma, and others. Our experience allows us to develop multiple bus models for in a fraction of the time it would take to do them individually.

For More Information...

Please contact one of our technically adept sales representatives today for a free, no obligation estimate for creating the bus models for your architecture.

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